11. [Once Amended] A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain [regions] region; and

a floating gate separated from the channel region by an insulator, wherein a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV.

18. [Once Amended] The transistor of claim 17, wherein the area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than the area of a capacitor formed by the floating gate, the insulator, and the channel region.

~~19.~~ [Once Amended] A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region; and

a floating gate separated from the channel region by an insulator, wherein a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

a control electrode, separated from the floating gate by an intergate dielectric;

[The transistor of claim 17,] wherein the intergate [insulator] dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

Please add new claims 28-32:

~~28.~~ [New] A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region;

a floating gate separated from the channel region by an insulator;

a control electrode, separated from the floating gate by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

29. [New] A memory cell comprising:

a storage electrode for storing charge;

a control electrode, separated from a storage electrode by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

30. [New] A method comprising:

selecting a memory cell using a control electrode of a floating gate transistor, wherein the control electrode is separated from a floating gate of the floating gate transistor by an intergate dielectric;

storing data by changing a charge of the floating gate;

reading data by detecting a current between a source and a drain of the floating gate transistor; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

31. [New] A method comprising:

forming a source region and a drain region of a floating gate transistor;

forming a gate insulator and a floating gate of the floating gate transistor;

forming a control gate of the floating gate transistor;

selecting an intergate dielectric material having a permittivity that is higher than a permittivity of silicon dioxide; and

forming an intergate dielectric from the intergate dielectric material in between the control gate and the floating gate.

32. [New] A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator;

a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

REMARKS

In response to the Office Action mailed September 3, 1998, Applicant has amended the claims of the above-identified patent application. Specifically, Applicant has deleted non-elected claims 21-26, amended claims 11 and 18-19 and added new claims 28-32 to more carefully claim the present invention. Reconsideration of the objections and the rejections, consideration of the new claims and allowance of all the pending claims is respectfully solicited.

INTERVIEW SUMMARY

Applicant's representative, Bradley Forrest, received a telephone restriction requirement from Examiner Valencia Wallace on August 18, 1998. Applicant's representative elected to prosecute claims 1-20 and 27 without traverse.